

## HAT3004R

Silicon N Channel / P Channel Power MOS FET  
High Speed Power Switching

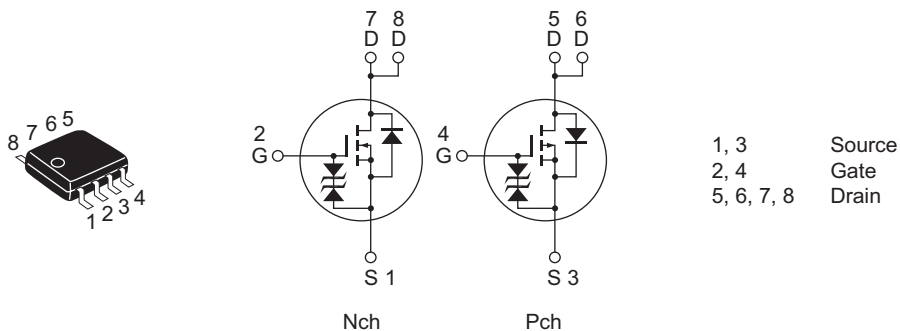
REJ03G1196-1100  
(Previous: ADE-208-500I)  
Rev.11.00  
Sep 07, 2005

### Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

### Outline

RENESAS Package code: PRSP0008DD-D  
(Package name: SOP-8 <FP-8DAV> )



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value		Unit
		Nch	Pch	
Drain to source voltage	$V_{DSS}$	30	-30	V
Gate to source voltage	$V_{GSS}$	±20	±20	V
Drain current	$I_D$	5.5	-3.5	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	44	-28	A
Body-drain diode reverse drain current	$I_{DR}$	5.5	-3.5	A
Channel dissipation	$P_{ch}$ <sup>Note 2</sup>	2		W
Channel dissipation	$P_{ch}$ <sup>Note 3</sup>	3		W
Channel temperature	$T_{ch}$	150		°C
Storage temperature	$T_{stg}$	-55 to +150		°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$ 2. 1 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm),  $PW \leq 10 s$ 3. 2 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm),  $PW \leq 10 s$ 

## Electrical Characteristics

### N Channel

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 mA, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = \pm 16 V, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	μA	$V_{DS} = 30 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$V_{DS} = 10 V, I_D = 1 mA$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.050	0.065	Ω	$I_D = 3 A, V_{GS} = 10 V$ <sup>Note 4</sup>
	$R_{DS(on)}$	—	0.078	0.11	Ω	$I_D = 3 A, V_{GS} = 4 V$ <sup>Note 4</sup>
Forward transfer admittance	$ y_{fs} $	3.5	5.5	—	S	$I_D = 3 A, V_{DS} = 10 V$ <sup>Note 4</sup>
Input capacitance	$C_{iss}$	—	310	—	pF	$V_{DS} = 10 V$
Output capacitance	$C_{oss}$	—	220	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	100	—	pF	$f = 1 MHz$
Turn-on delay time	$t_{d(on)}$	—	17	—	ns	$V_{GS} = 4 V, I_D = 3 A$
Rise time	$t_r$	—	190	—	ns	$V_{DD} \cong 10 V$
Turn-off delay time	$t_{d(off)}$	—	25	—	ns	
Fall time	$t_f$	—	60	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.9	1.4	V	$I_F = 5.5 A, V_{GS} = 0$ <sup>Note 4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	50	—	ns	$I_F = 5.5 A, V_{GS} = 0$ $di_F/dt = 20 A/\mu s$

Note: 4. Pulse test

## P Channel

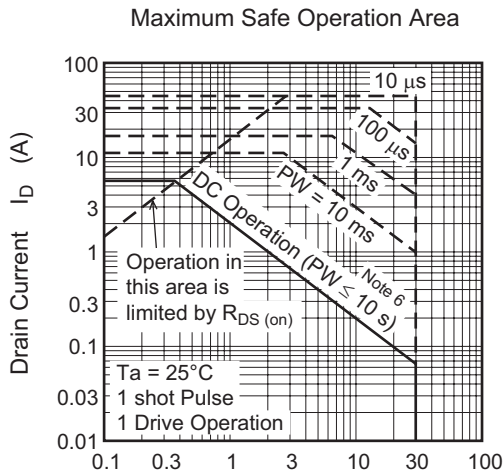
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-10	$\mu\text{A}$	$V_{DS} = -30 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$ , $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	$\Omega$	$I_D = -2 \text{ A}$ , $V_{GS} = -10 \text{ V}$ <sup>Note 5</sup>
	$R_{DS(on)}$	—	0.20	0.34	$\Omega$	$I_D = -2 \text{ A}$ , $V_{GS} = -4 \text{ V}$ <sup>Note 5</sup>
Forward transfer admittance	$ y_{fs} $	2.5	3.5	—	S	$I_D = -2 \text{ A}$ , $V_{DS} = -10 \text{ V}$ <sup>Note 5</sup>
Input capacitance	$C_{iss}$	—	350	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	$C_{oss}$	—	230	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	75	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	18	—	ns	$V_{GS} = -4 \text{ V}$ , $I_D = -2 \text{ A}$
Rise time	$t_r$	—	110	—	ns	$V_{DD} \equiv -10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	20	—	ns	
Fall time	$t_f$	—	30	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	-1.0	-1.5	V	$I_F = -3.5 \text{ A}$ , $V_{GS} = 0$ <sup>Note 5</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	60	—	ns	$I_F = -3.5 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 20 \text{ A}/\mu\text{s}$

Note: 5. Pulse test

# Main Characteristics

## N Channel

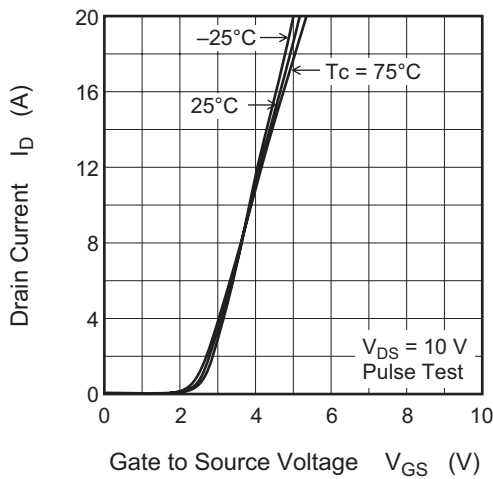


Drain to Source Voltage  $V_{DS}$  (V)

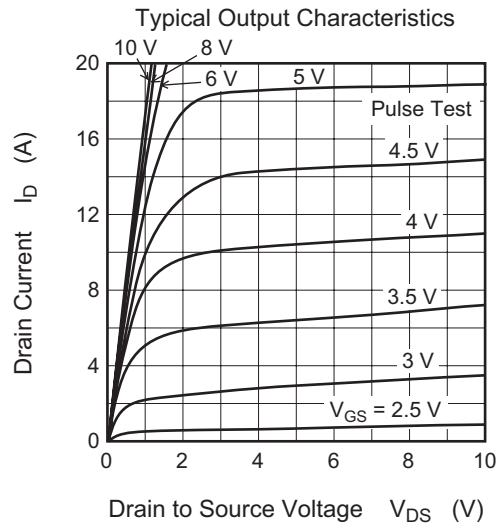
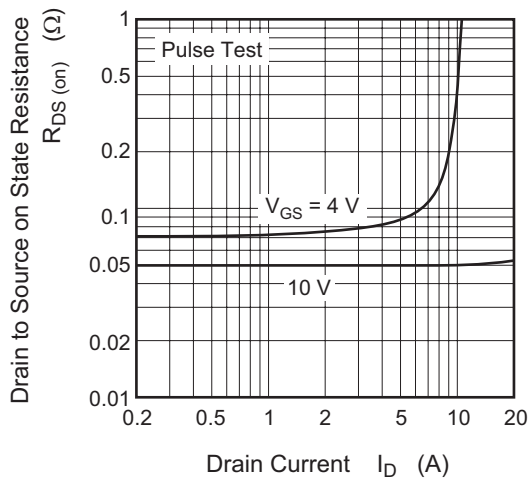
Note 6:

When using the glass epoxy board (FR4 40 × 40 × 1.6 mm)

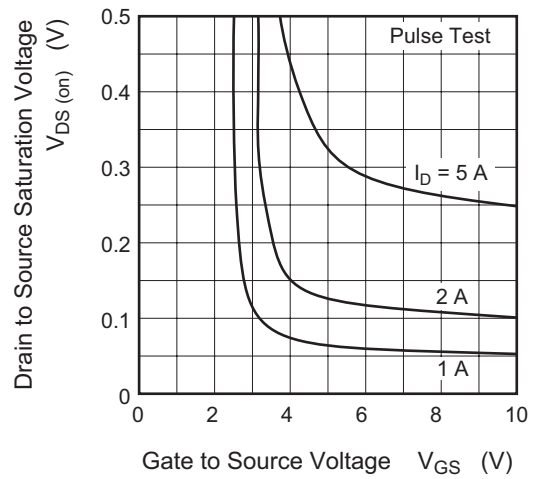
Typical Transfer Characteristics



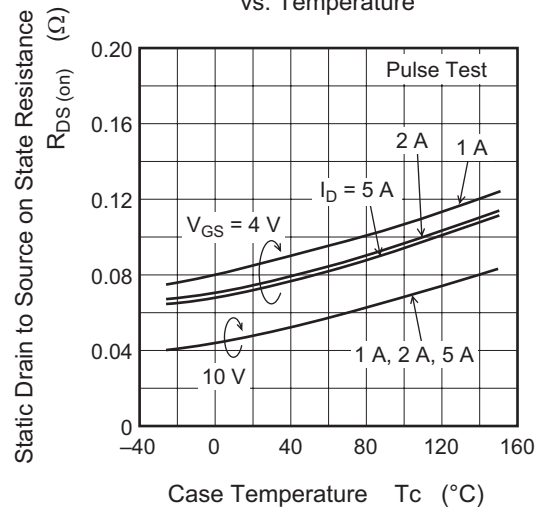
Static Drain to Source on State Resistance vs. Drain Current

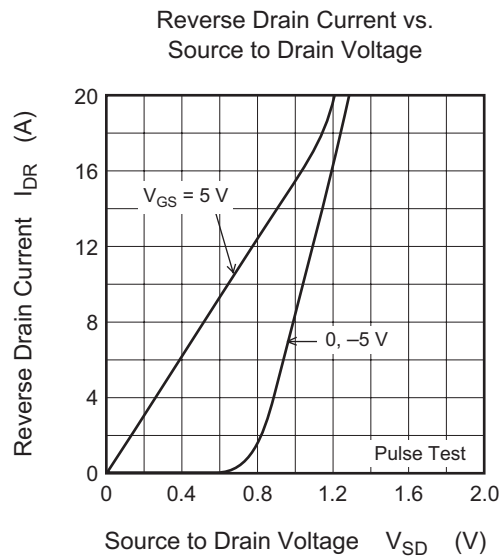
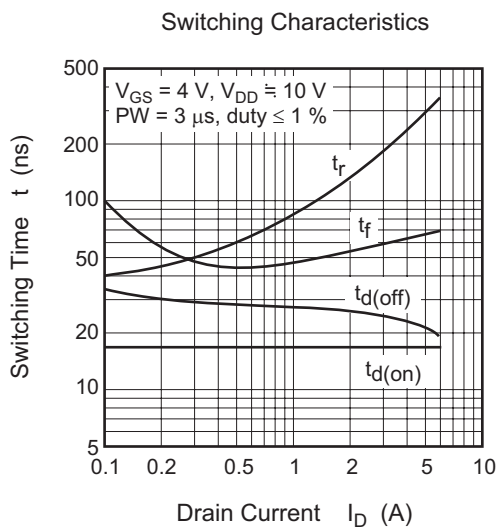
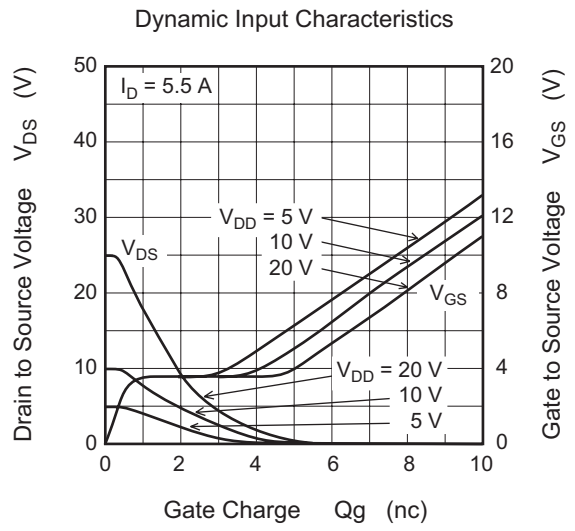
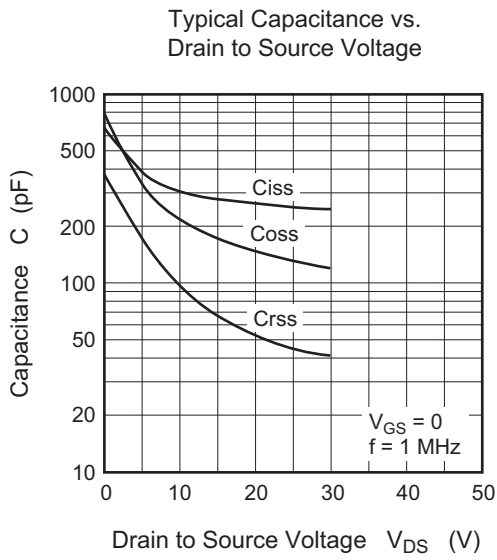
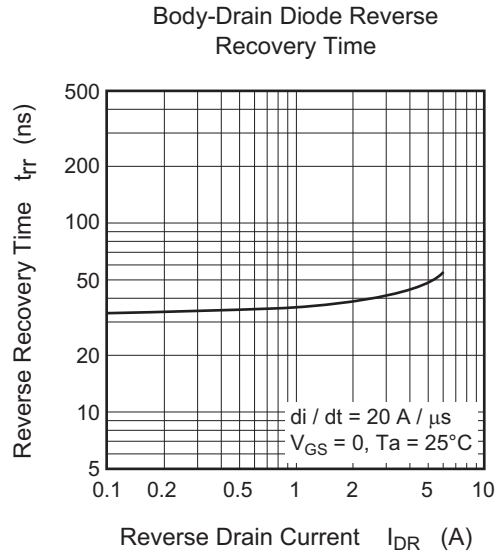
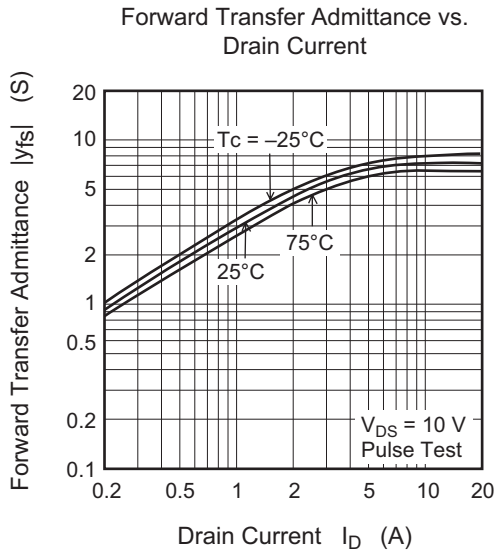


Drain to Source Saturation Voltage vs. Gate to Source Voltage



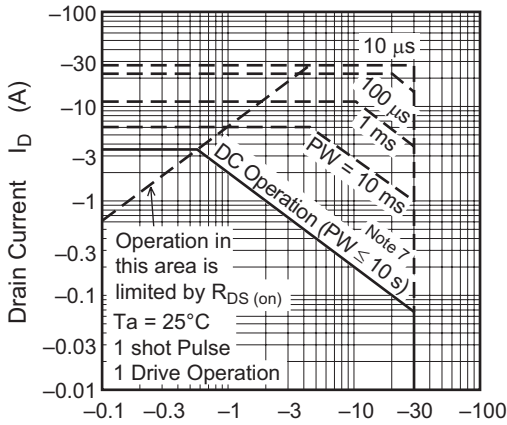
Static Drain to Source on State Resistance vs. Temperature





P Channel

Maximum Safe Operation Area

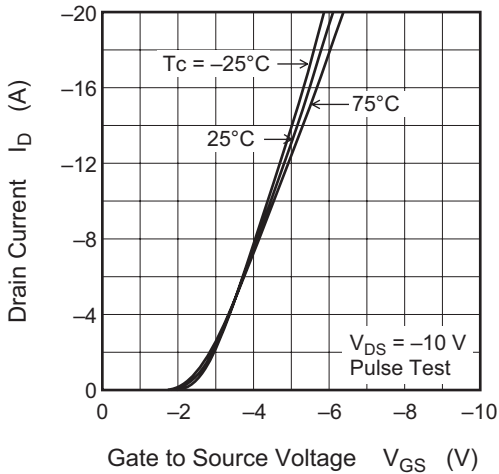


Drain to Source Voltage  $V_{DS}$  (V)

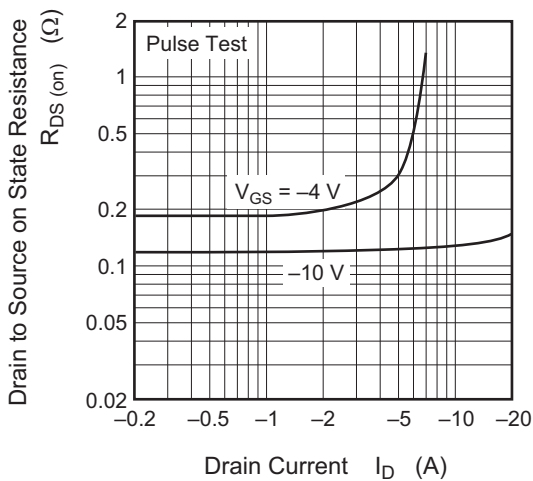
Note 7:

When using the glass epoxy board (FR4 40 × 40 × 1.6 mm)

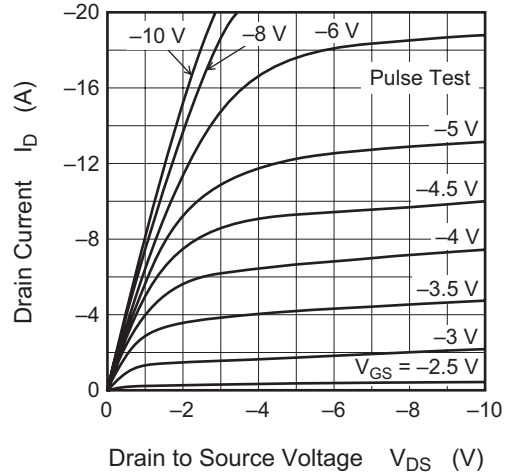
Typical Transfer Characteristics



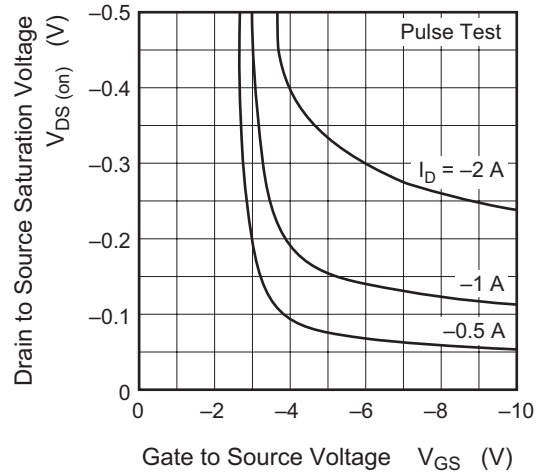
Static Drain to Source on State Resistance vs. Drain Current



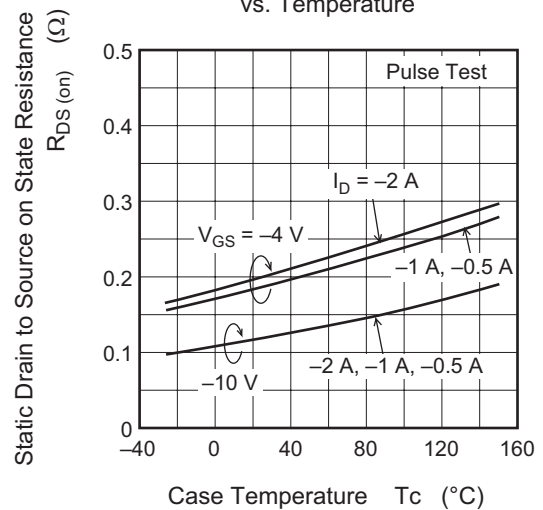
Typical Output Characteristics

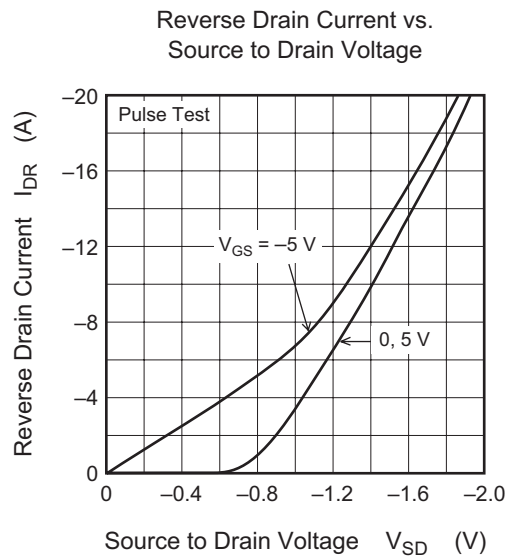
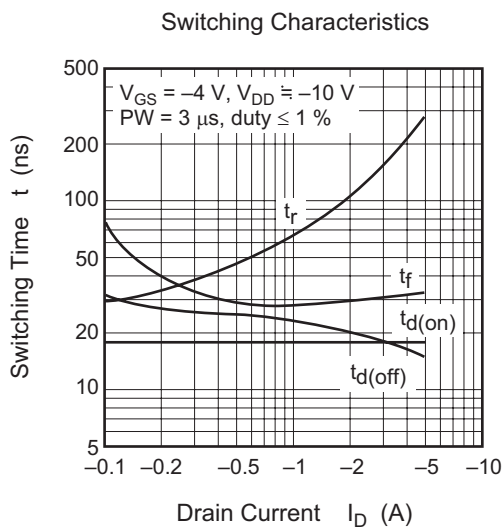
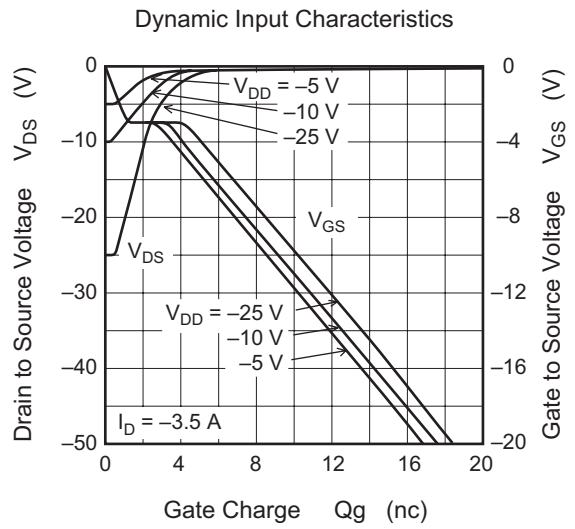
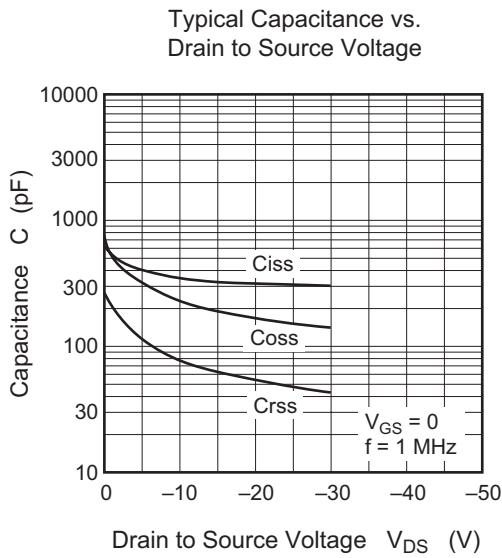
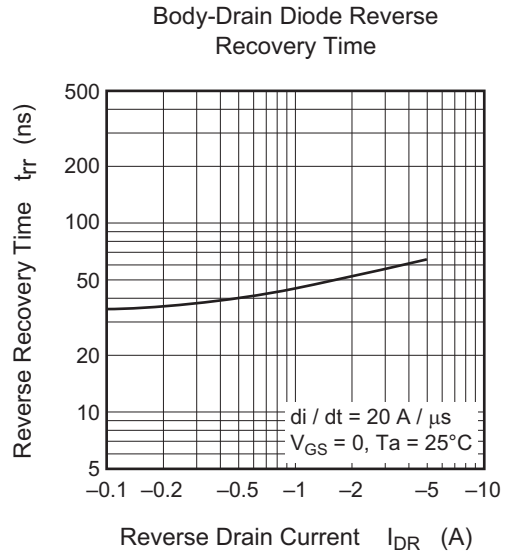
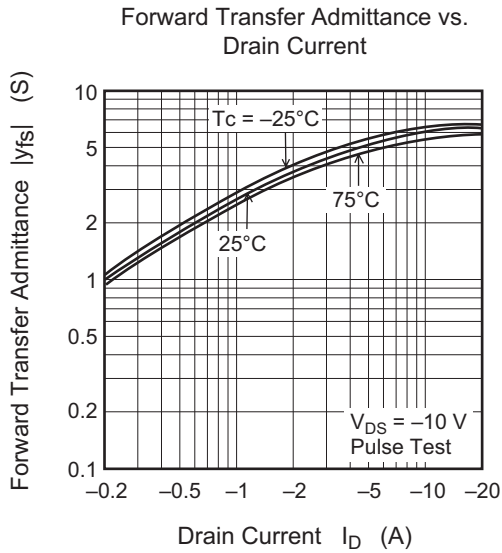


Drain to Source Saturation Voltage vs. Gate to Source Voltage

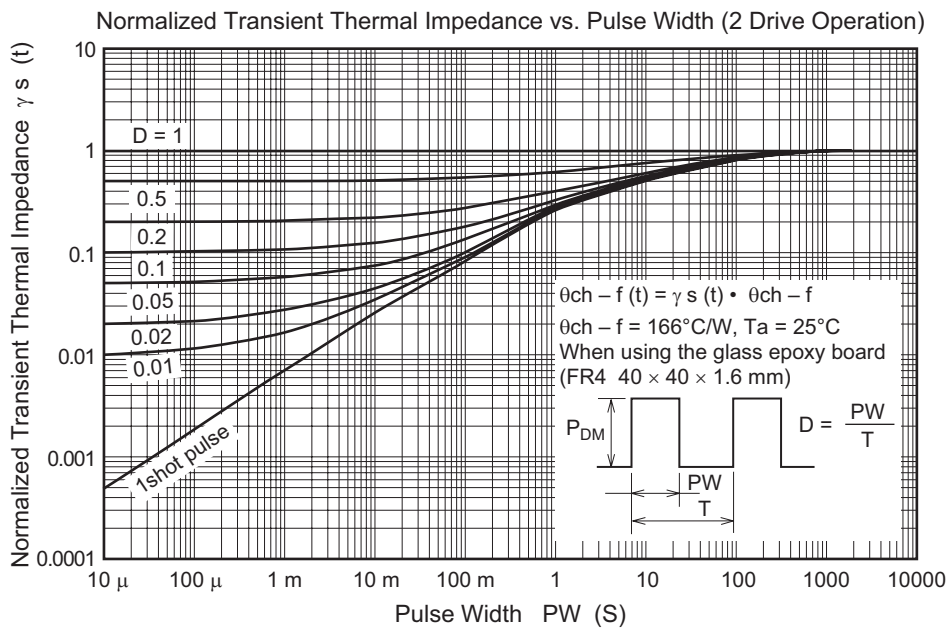
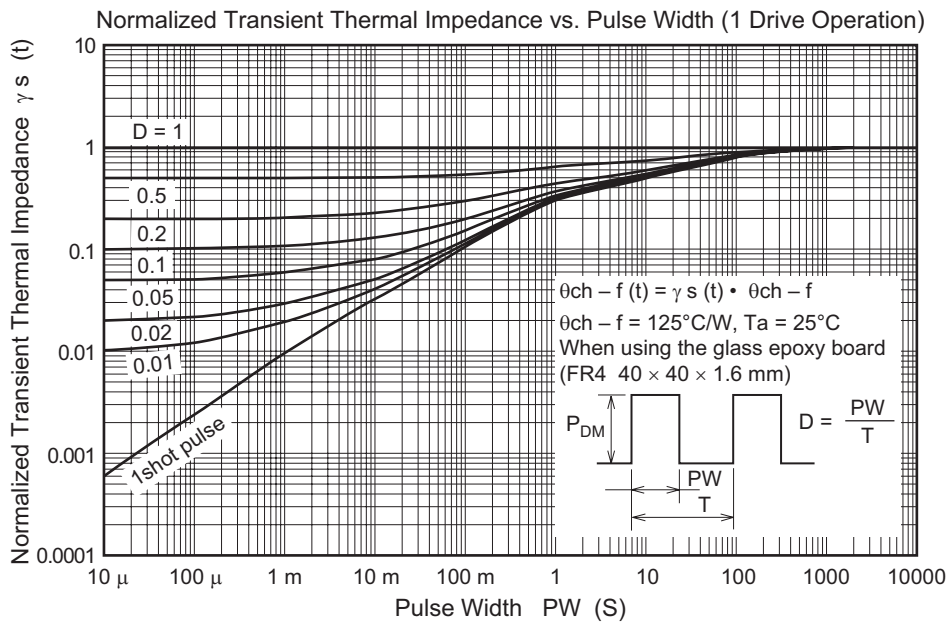
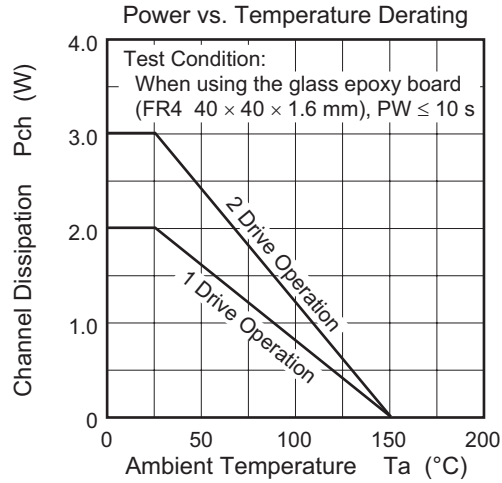


Static Drain to Source on State Resistance vs. Temperature





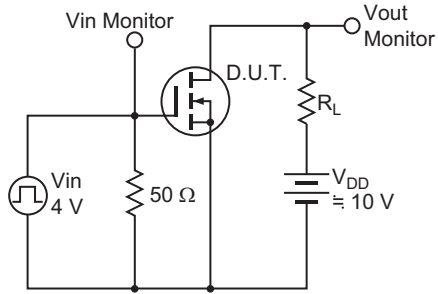
Common



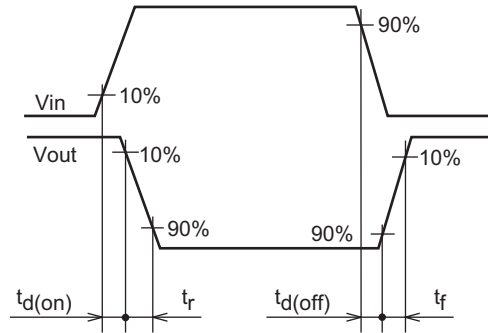


N channel

Switching Time Test Circuit

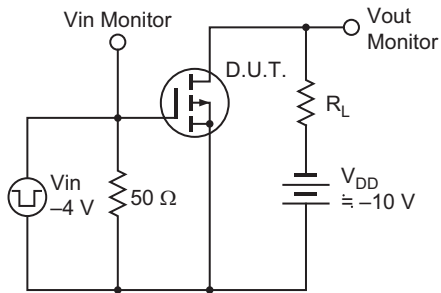


Switching Time Waveform

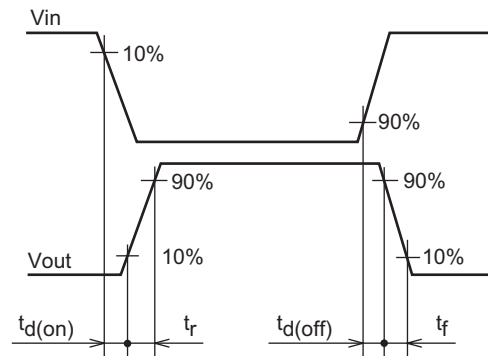


P channel

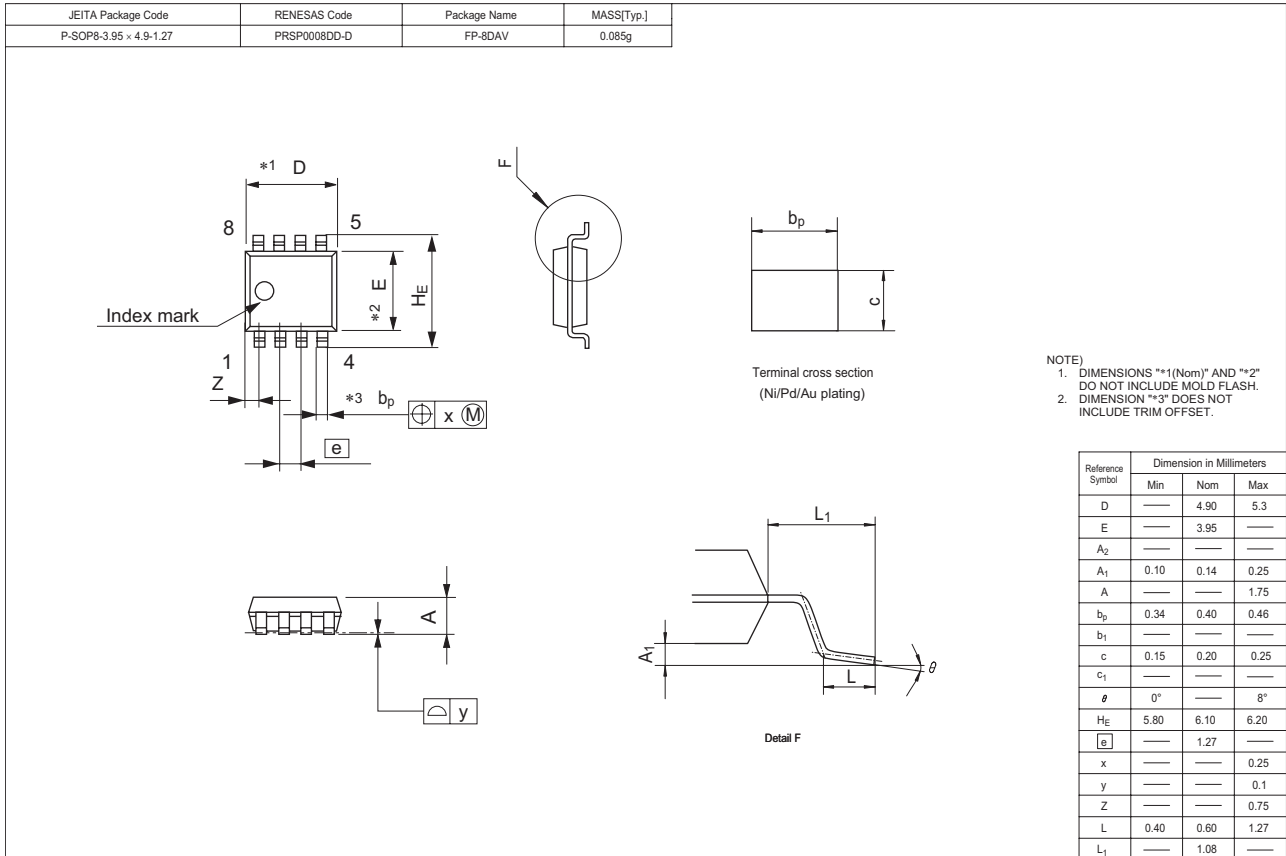
Switching Time Test Circuit



Switching Time Waveform



### Package Dimensions



### Ordering Information

Part Name	Quantity	Shipping Container
HAT3004R-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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